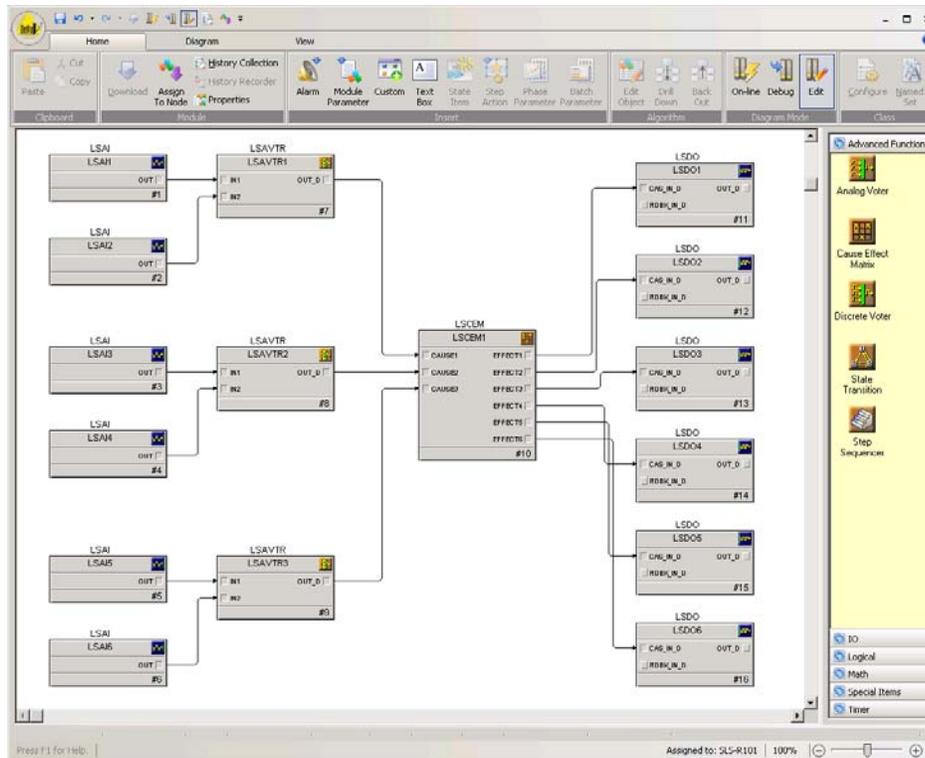


DeltaV SIS™ Function Blocks



DeltaV SIS function blocks provide an easy, yet powerful configuration environment.

- Certified for use in SIL 3 applications
- Powerful functionality, yet easy to use
- Includes integrated change management

A rich set of smart function blocks has been designed specifically for the DeltaV SIS platform. These reduce what formerly took pages of ladder logic and custom programming to engineer into a simple drag-and-drop configuration activity, with built-in change management for easy adherence to the IEC 61511 standard.

Introduction

A standards-based approach makes the configuration environment of the DeltaV SIS system unique. Certified to comply with IEC 61508, the function blocks are designed to make the implementation and management of the safety configuration as efficient as possible.

The set of advanced function blocks is certified by TÜV for safety applications.

Other capabilities making the DeltaV SIS software easy to engineer include:

The DeltaV SIS system shares the same configuration environment as the industry-leading DeltaV system and includes all of the same advances in ease of use, like plug-and-play hardware, drag-and-drop configuration and explorer-based software.

- Built-in alarm state engine per EEMUA 191 standard
- Off-line simulation

Benefits

Certified for use in SIL 3 applications

All of the DeltaV SIS function blocks have been certified for use in SIL 3 applications without exception. The library of function blocks has been carefully designed to provide the safety functionality that is required in today's SIS environment, while eliminating the riskier approach to configuration that is often seen in older systems, such as pages of hard-to-verify ladder logic or the need to translate a Cause and Effect Matrix into code.

Powerful functionality, yet easy to use

The blocks have been designed to combine industry-leading functionality with the ease-of-use of a modern DCS. DeltaV SIS function blocks are built to the IEC 61131-3 function block diagrams standard and certified by TÜV, making safety logic development both intuitive and easy.

The real-world requirements of managing a process plant safely have also been addressed. For instance, you need to be sure that the valve will perform on demand. You need to decrease the test frequency of the safety functions from six months to the turnaround scheduled every six years. DeltaV SIS platform provides tools such as scheduled partial stroke testing of valves to meet these requirements. An alarm is generated on partial stroke failure or advanced diagnostic alert detection and the valve is available on demand even while the partial stroke test is in progress.

Voter function blocks provide advanced features like built-in bypasses and deviation alarms to improve plant availability. The voting is configured using radio buttons and check-boxes, with extensible blocks ensuring that the same approach is taken throughout the configuration, regardless of the scale of the application in question.

With optionally certified Rosemount transmitters and Fisher Digital Valve Controller, DeltaV SIS system and the AMS Device Manager, the architecture is in place. With patented DeltaV SIS function blocks, each one specifically designed to meet an industry need, configuration is a few mouse clicks away. With Control Studio and powerful function blocks, the Safety Integrity Level of the Safety Instrumented Function can be maintained with reduced field tests.

Integrated change management

Built on the experience of satisfying tough change management regulatory requirements, DeltaV SIS platform incorporates this change management to automate your IEC 61511 compliance. All changes in the DeltaV SIS logic are may be captured based on the change, who made it, and when it was made.

DeltaV SIS system also documents the changes to existing SIS logic, showing the nature of the change in addition to the identity of the person changing it. Where required by the standard, editing and verification are required to be by appropriately qualified personnel. These qualifications, including peer groupings and authorities to ensure that reviews have been made by the right people, are built-in from the start of the project.

Product Description

DeltaV SIS Function Blocks

These function blocks are allowed to execute within the DeltaV SIS logic solver (SLS 1508).

Function	Description
	<p>Analog Voter (LSAVTR)</p> <p>Compares the inputs against a configured limit to determine the output. If an input is greater than the configured limit the block counts that as a vote to set the output to Tripped. If the required number of inputs votes to trip, the output of the block goes to tripped value.</p>
	<p>Discrete Voter (LSDVTR)</p> <p>Reads each input to determine if it is a vote to trip or not. If the required number of inputs is voting to trip, the output goes to the tripped value.</p>
	<p>Cause And Effect Matrix (LSCEM)</p> <p>Executes interlock and permissive logic to associate as many as 16 inputs (causes) with as many as 16 outputs (effects) to control one or more final elements.</p>
	<p>State Transition Diagram (LSSTD)</p> <p>Implements a state machine. The block changes state based on the values of its transition inputs.</p>
	<p>Step Sequencer (LSSEQ)</p> <p>Drives a number of discrete block outputs based on the input sequence number.</p>
	<p>Analog Input (LSAI)</p> <p>Reads a single analog signal from an analog input channel and makes it available to other function blocks. The function block performs scaling and provides a square root function for the input data. Analog inputs can be from conventional or HART channels. This function block does not use digital values from HART channels.</p>
	<p>Discrete Input (LSDI)</p> <p>Reads a single discrete input from a two-state field device and makes the processed physical input available to other function blocks. You can configure inversion on the input value.</p>
	<p>Discrete Output (LSDO)</p> <p>Drives a logic solver discrete output channel to manipulate a solenoid or other final element.</p>
	<p>Digital Valve Controller (LSDVC)</p> <p>Connects to Fisher digital valve controllers (DVC 6000 SIS) via a logic solver HART 2-state output channel. Contains all of the parameters found in the Discrete output block plus a set of additional parameters used for partial stroke testing.</p>
	<p>Alarm (LSALM)</p> <p>Performs alarm detection on an input. Because the block allows easy access to analog channel data in the Logic Solver, you can choose when alarms are appropriate instead of associating alarming with I/O function blocks.</p>
	<p>Limit (LSLIM)</p> <p>Limits an input value between two reference values. The block has options that set the output to a default value or the last value if the input becomes out of range.</p>

Function	Description
	<p>Comparator (LSCMP) Compares two values and sets a Boolean output based on that comparison. Comparisons are Less Than, Greater Than, Equal To, Not Equal. The block can also compare the input value against a range to determine if the input is in range.</p>
	<p>Middle Signal Select (LSMID) Selects between multiple analog signals. This block selects the mid-valued input from those inputs that are not bad. When there is an even number of inputs in the selection process, the average of the 2 mid-valued inputs is used as the middle value</p>
	<p>Boolean Fan Input (LSBFI) Decodes a binary weighted input to individual bits and generates a discrete output value for each bit.</p>
	<p>Boolean Fan Output (LSBFO) Decodes a binary weighted input to individual bits and generates a discrete output value for each bit.</p>
	<p>Bi-directional Edge Trigger (LSBDE) Generates a True (1) discrete pulse output when the discrete input makes a positive (False-to-True) or a negative (True-to-False) transition since the last execution of the block. If there has been no transition, the discrete output is False (0).</p>
	<p>Positive Direction Edge Trigger (LSPDE) Generates a True (1) discrete pulse output when the discrete input makes a positive (False-to-True) transition since the last execution of the block. If there has been no transition, the discrete output is False (0).</p>
	<p>Negative Direction Edge Trigger (LSNDE) Generates a True (1) discrete pulse output when the discrete input makes a negative (True-to-False) transition since the last execution of the block. If there has been no transition, the discrete output is False (0).</p>
	<p>Reset/Set Flip-flop (LSRS) Generates a discrete output value based on NOR logic of reset and set inputs. If the reset input is False (0) and the set input is True (1), the output is True. The output remains True regardless of the set value until the reset value is True. When reset becomes True, the output is False. When both inputs are True, the output is False. When both inputs become False, the output remains at its last state and can be either True or False.</p>
	<p>Set/Reset Flip-flop (LSSR) Generates a discrete output value based on NAND logic of set and reset inputs. When the reset input is False (0) and the set input is True (1), the output is True. The output remains True until the reset input is True and the set input is False. When the reset input is True, the output is equal to the set input. When both inputs are True, the output is True. When both inputs become False, the output remains at its last state and can be either True or False.</p>
	<p>Logical And (LSAND), Not And (LSNAND) AND—Generates a discrete output value based on the logical AND of two to sixteen discrete inputs. NAND—Generates a discrete output value based on inverting the logical AND of two to sixteen discrete inputs.</p>

Function	Description
	<p>Logical Or (LSOR), Not OR (LSNOR)</p> <p>OR—Generates a discrete output value based on the logical OR of two to sixteen discrete inputs. When one or more of the inputs is True (1), the output is set to True.</p> <p>NOR—Generates a discrete output value based on inverting the logical OR of two to sixteen discrete inputs. When one or more of the inputs is True (1), the output is set to False.</p>
	<p>Not (LSNOT)</p> <p>Inverts a discrete input signal. Supports signal status propagation.</p>
	<p>Logical Not Exclusive Or (LSXNOR), Exclusive OR (LSOR)</p> <p>XOR—Performs an exclusive OR of two inputs to produce a discrete output.</p> <p>XNOR—Inverts the result of an exclusive OR of two inputs.</p>
	<p>Off Delay Timer (LSOFFD)</p> <p>Delays the transfer of a False (0) discrete input value to the output by a specified time period.</p>
	<p>On-Delay Timer (LSOND)</p> <p>Delays the transfer of a True (1) discrete input value to the output by a specified time period.</p>
	<p>Retentive Timer (LSRET)</p> <p>Generates a True (1) discrete output after the input has been True for a specified time period. The elapsed time the input has been True and the output value are reset when the reset input is set True.</p>
	<p>Timed Pulse (LSTP)</p> <p>Generates a True (1) discrete output for a specified time duration when the input makes a positive (False-to-True) transition. The output remains True even when the input returns to its initial discrete value and returns to its original False value only when the output is True longer than the specified time duration. Any 0 to True transition causes the timer to reset.</p>
	<p>Calculation/Logic (LSCALC)</p> <p>Evaluates a structured text expression.</p>

Ordering Information

Description	Model Number
ProfessionalPLUS Station	VE2101S xxxxx*

* xxxxx = 00025 to 30000 DST(s) - The license limits are enforced on a system-wide basis and not on a per logic solver basis. For details refer to the SIS Licensing whitepaper.

Prerequisites

- DeltaV v8.3 software or later.

To locate a sales office near you, visit our website at:

www.DeltaVSIS.com

Or call us at:

Asia Pacific: 65.777.8211

Europe, Middle East: 41.41.768.6111

North America, Latin America: +1 800.833.8314 or
+1 512.832.3774

For large power, water, and wastewater applications

contact Power and Water Solutions at:

www.EmersonProcess-powerwater.com

Or call us at:

Asia Pacific: 65.777.8211

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North America, Latin America: +1 412.963.4000

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